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TESTA, HURWITZ & THIBEAULT, LLP
HIGH STREET TOWER
125 HIGH STREET
BOSTON, MA 02110

EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/871,180	Applicant(s) TETREAULT, MARK	
	Examiner Michael C Maskulinski	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-29* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Office Action

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-4, 6-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Buckland et al., U.S. Patent 5,815,647.

Referring to claim 1:

a. In column 12, lines 24-28, Buckland et al. disclose that the device driver has the responsibility for checking the status of any I/O operations at either the bridge chip or the device itself to make sure that the operation is completed correctly at specific points in the code (bus interface logic in communication with the bus, the bus interface logic generating a signal indicating the status of the bus).

b. In column 12, lines 15-20, Buckland et al. disclose that a status bit in a register is set to signal an external interrupt to the system. Also, when the configuration bit is set (an isolation switch in communication with the bus), any further loads or stores from the CPU to the device are ignored by throwing away any data from the CPU on a store, and returning a value of all logical ones on any load operated.

c. In column 12, lines 61-67, Buckland et al. disclose determining whether an SERR# signal is present from one of the plurality of devices on the adapter cards in the computer system. If so, then the reset signal RST# is activated (by bridge chip) to the device signaling SERR#, to place the device in its reset state and

avoid any damage to the system, while still keeping the device coupled to the system (isolation control logic in communication with the bus interface logic and the isolation switch, wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal). Further, in column 6, lines 45-63, Buckland et al. disclose that each slot can be selectively rest with a RST# signal as indicated by a user, and power removed from the slot when an I/O card is to be removed, replaced, or installed (a received device isolation signal).

Referring to claim 2, in column 11, lines 63-65, Buckland et al. disclose a register that is added to the bridge chip for storing status information (the bus interface logic comprises a state machine).

Referring to claim 3, although Buckland et al. don't explicitly disclose that the bus interface logic comprises combinatorial logic, it is inherent to the system of Buckland et al. In column 12, lines 9-12, Buckland et al. disclose a recovery mode configuration bit is added that will be set when any error condition is present on a particular one of the cards in a slot. Combinatorial logic is necessary to set a bit in a digital system.

Referring to claim 4, in column 12, lines 55-67, Buckland et al. disclose the bridge chip monitors the bus for the SERR# signal (the bus interface logic monitors all bus transactions).

Referring to claim 6, although Buckland et al. don't explicitly disclose that the isolation control logic comprises combinatorial logic, it is inherent to the system of

Buckland et al. Combinatorial logic is necessary for extracting the configuration bit (see column 12, lines 5-23).

Referring to claim 7, in column 12, lines 24-41, Buckland et al. disclose that the device driver has responsibility for checking the status of any I/O operations at either the bridge chip, or the device itself to make sure that the operation is completed correctly at specific points in the code (instructions being executed). A register will contain some bit where, e.g. a logical 0 will indicate that there is no error present and the device driver can read the information from the I/O device. However, if the status bit in the register contains a logical 1 and the bridge chip is holding the device in the reset state (RST# active), then when the device driver reads the information from the device all the bits will be set to logical ones, thus, indicating to the driver that the operation did not complete properly (wherein the isolation control logic receives the device isolation signal from logic monitoring the operational status of the system).

Referring to claims 8 and 9, in column 2, lines 63-65, Buckland et al. disclose a flow chart for hot plugging adapter cards into the I/O slots. Further, in column 7, lines 47-67 continued in column 8, lines 1-16, Buckland et al. disclose an electromechanical sensing device that provides the card presence signal (the hot-plug logic element generates the device isolation signal responsive to the physical removal of the device from its slot). A process will determine that a card exists in the slot, since it is being assumed that a card is being removed. The user will initiate this process by inputting commands, or the like to the computer system, via a keyboard, mouse, stylus, or other I/O device. These commands may require the user to provide certain information, such

as which one of a plurality of slots is to be re-configured, or the like. At the next step, the operating system, such as the Disk Operating System (DOS), OS/2, AIX, or the like (OS/2 and AIX are trademarks of IBM Corp.) causes all data processing activity between the adapter and the remainder of the computer system to be ceased. Subsequently, a reset RST# signal is issued from the bridge chip to the I/O slot. The RST# signal is also sent to reset detector, which in turn transmits a control signal to bridge control logic. Then, the I/O bridge chip decouples the secondary bus from the primary I/O bus. This decoupling is accomplished by a control signal, which is sent from bridge control logic to the I/O bridge chip. Based on the detection of the RST# signal slot reset detector also sends a control signal to the power control logic, indicating that the power to the slot should be gradually reduced (ramped down). The power is then decreased (the isolation control logic receives the device isolation signal from a hot-plug logic element).

Referring to claims 10 and 11, in column 11, lines 2-3, Buckland et al. disclose that address parity errors are reported with a system error signal (SERR#). Further, in column 12, lines 61-67, Buckland et al. disclose determining whether an SERR# signal is present from one of the plurality of devices on the adapter cards in the computer system. If so, then the reset signal RST# is activated (by bridge chip) to the device signaling SERR#, to place the device in its reset state and avoid any damage to the system, while still keeping the device coupled to the system (the isolation control logic receives the device isolation signal from protocol checker logic monitoring the validity of bus transactions).

Referring to claim 12, on a PCI bus it is inherent that the bus transactions are communicated on the bus in relation to clock cycles.

3. Claims 1, 2, 4, 5, 7-10, and 14-29 rejected under 35 U.S.C. 102(b) as being anticipated by Goodrum et al., U.S. Patent 6,032,271.

Referring to claim 1:

a. In column 1, lines 40-41, Goodrum et al. disclose a watcher that includes a bus timer to monitor the bus to detect the bus hang condition (bus interface logic in communication with the bus, the bus interface logic generating a signal indicating the status of the bus).

b. In column 1, lines 28-31, Goodrum et al. disclose a fault isolation controller that includes circuitry for turning off the devices when a faulty condition is detected (an isolation switch in communication with the bus).

c. In column 1, lines 28-31, Goodrum et al. disclose a fault isolation controller (isolation control logic in communication with the bus interface logic and the isolation switch).

d. In column 1, lines 37-45, Goodrum et al. disclose that the fault isolation controller is used to turn devices off by powering them off. The devices are coupled to a bus, and the faulty condition includes a bus hang condition. The watcher includes a bus timer to monitor the bus to detect the bus hang condition. The bus hang condition is present if the bus timer expires. The fault isolation controller is used to turn off the devices when the bus hang condition is detected and to turn the devices back on to test the device (wherein the isolation control

logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal). Further, in column 2, lines 33-37, Goodrum et al. disclose that the illegal condition occurs when a PCI signal TRDY_, STOP_, or DEVSEL_ is asserted during a bus idle condition (a received device isolation signal).

Referring to claim 2, in column 1, lines 52-53, Goodrum et al. disclose that the watcher includes a storage device for storing information on the bus associated with the faulty condition (the bus interface logic comprises a state machine).

Referring to claim 4, in column 1, lines 40-41, Goodrum et al. disclose a watcher that includes a bus timer to monitor the bus to detect the bus hang condition (the bus interface logic monitors all bus transactions).

Referring to claims 5 and 14, in column 1, lines 26-59, Goodrum et al. teach detecting a bus hang condition by monitoring a watchdog timer indicating that there hasn't been any activity on the bus (the bus status signal generated by the bus interface logic indicates that the bus is idle).

Referring to claim 7, in column 1, lines 37-45, Goodrum et al. disclose that the fault isolation controller is used to turn devices off by powering them off. The devices are coupled to a bus, and the faulty condition includes a bus hang condition. The watcher includes a bus timer to monitor the bus to detect the bus hang condition. The bus hang condition is present if the bus timer expires. The fault isolation controller is used to turn off the devices when the bus hang condition is detected and to turn the

devices back on to test the device (the isolation control logic receives the device isolation signal from logic monitoring the operational status of the system).

Referring to claims 8 and 9, in column 69, line 16 through column 71, line 30, Goodrum et al. teach that the isolation control logic receives the device isolation signal from a hot-plug logic element and that the hot-plug logic element generates the device isolation signal responsive to the physical removal of the device from the slot.

Referring to claim 10, in column 2, lines 29-32, Goodrum et al. disclose that the invention features a computer system having a bus, a watcher for detecting an illegal condition on the bus and a storage device for storing information on the bus associated with the illegal condition (the isolation control logic receives the device isolation signal from protocol checker logic monitoring the validity of bus transactions).

Referring to claim 15, in column 1, lines 40-41, Goodrum et al. disclose a watcher that includes a bus timer to monitor the bus to detect the bus hang condition (a timer measuring elapsed time).

Referring to claim 16, in column 87, lines 41-50, Goodrum et al. teach that the timer measures elapsed time relative to a system event.

Referring to claim 17, in column 87, lines 43-44, Goodrum et al. disclose that if the watchdog timer expires, then the bus has hung (a timeout signal is generated in response to the elapsed time exceeding a predetermined threshold).

Referring to claim 18, in column 87, lines 51-55, Goodrum et al. disclose that when the watchdog timer expires, the bus hang pending bit is set active in the bus-hang indication register. When set active, the bus hang pending bit disables the bus watcher.

Next, the slot enable bits in the SIO are cleared, causing the slots to be powered off. Further, in column 88, lines 23-35, Goodrum et al. disclose resetting the bus so that the bus watcher can be re-enabled (the isolation control logic transmits a bus reset signal responsive to receiving both the device isolation signal and the timeout signal from the timer).

Referring to claims 19 and 24:

a. In column 1, lines 28-31, Goodrum et al. disclose a fault isolation controller that includes circuitry for turning off the devices when a faulty condition is detected (receiving a signal identifying a bus device to be isolated, the bus device performing a bus transaction).

b. In column 1, lines 40-41, Goodrum et al. disclose a watcher that includes a bus timer to monitor the bus to detect the bus hang condition (receiving a bus status signal).

c. In column 1, lines 37-45, Goodrum et al. disclose that the fault isolation controller is used to turn devices off by powering them off. The devices are coupled to a bus, and the faulty condition includes a bus hang condition. The watcher includes a bus timer to monitor the bus to detect the bus hang condition. The bus hang condition is present if the bus timer expires. The fault isolation controller is used to turn off the devices when the bus hang condition is detected and to turn the devices back on to test the device (wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal). Further, in column 2, lines 33-37,

Goodrum et al. disclose that the illegal condition occurs when a PCI signal TRDY_, STOP_, or DEVSEL_ is asserted during a bus idle condition (a received device isolation signal).

Referring to claims 20 and 25, in column 1, lines 28-31, Goodrum et al. disclose a fault isolation controller that includes circuitry for turning off the devices when a faulty condition is detected (the step of isolating the identified bus device from the bus responsive to the received bus device isolation signal).

Referring to claims 21 and 27, in column 1, lines 37-38, Goodrum et al. disclose that the fault isolation controller is used to turn devices off by powering them off (the step of inhibiting bus access).

Referring to claims 22 and 28, in column 87, lines 41-50, Goodrum et al. disclose that the bus watcher includes a watchdog timer to determine whether the secondary bus has locked up (the bus status signal indicating that the bus is not idle). If the watchdog timer expires (receiving a timeout signal), then the bus has hung. Further, in column 88, lines 23-35, Goodrum et al. disclose resetting the bus so that the bus watcher can be re-enabled (resetting the bus responsive to receiving both the timeout signal and the bus status signal indicating that the bus is not idle).

Referring to claims 23 and 29, in column 90, lines 13-24, Goodrum et al. disclose that the bus hang recovery state machine ensures that the secondary PCI bus is brought back to the idle state to allow the software to isolate the faulty slot. When the hang condition is detected, the SIO powers down the secondary bus slots, which would automatically place the bus into the idle state if one of the slot devices was the bus

master when the hang condition occurred. However, if one of the slot devices was the target (and the bridge chip was the master) when the bus hang occurred, then the bridge chip would remain on the bus. To take the bridge chip off the bus, the recovery state machine forces a retry cycle on the PCI bus by asserting the signal STOP.sub (wherein step (b) comprises isolating the bus controller from the bus).

Referring to claim 26, in column 1, lines 28-31, Goodrum et al. disclose that the fault isolation controller includes circuitry for turning off the devices when a faulty condition is detected and turns the devices back on to test the devices (the bus device isolation means comprises an isolation switch).

Allowable Subject Matter

4. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed April 21, 2004 have been fully considered but they are not persuasive.

6. On page 5, under the section **Comparison of Claim 1 to Teachings of Buckland**, the Applicant argues, "Buckland does not teach an apparatus 'wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal and a received device isolation signal' (emphasis by Applicant) as recited in claim 1." The Examiner respectfully disagrees. In

column 12, lines 61-67, Buckland et al. disclose determining whether an SERR# signal is present from one of the plurality of devices on the adapter cards in the computer system. If so, then the reset signal RST# is activated (by bridge chip) to the device signaling SERR#, to place the device in its reset state and avoid any damage to the system, while still keeping the device coupled to the system (isolation control logic in communication with the bus interface logic and the isolation switch, wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal). Further, in column 6, lines 45-63, Buckland et al. disclose that each slot can be selectively rest with a RST# signal as indicated by a user, and power removed from the slot when an I/O card is to be removed, replaced, or installed (a received device isolation signal).

7. On page 7, under the section **Comparison of Claim 1 to Teachings of Goodrum**, the Applicant argues, "Goodrum does not teach an apparatus 'wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal and a received device isolation signal' (emphasis by Applicant) as recited in claim 1." The Examiner respectfully disagrees. In column 1, lines 37-45, Goodrum et al. disclose that the fault isolation controller is used to turn devices off by powering them off. The devices are coupled to a bus, and the faulty condition includes a bus hang condition. The watcher includes a bus timer to monitor the bus to detect the bus hang condition. The bus hang condition is present if the bus timer expires. The fault isolation controller is used to turn off the devices when the bus hang condition is detected and to turn the devices back on to test the device

(wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal). Further, in column 2, lines 33-37, Goodrum et al. disclose that the illegal condition occurs when a PCI signal TRDY_, STOP_, or DEVSEL_ is asserted during a bus idle condition (a received device isolation signal).

8. On page 8, under the section **Comparison of Claims 19 and 24 to Teachings of Goodrum**, the Applicant argues, "Goodrum does not teach a method for isolating the bus device from the bus that includes 'transmitting an isolation switch control responsive to both the received device isolation signal and the received bus status signal.'" The Examiner respectfully disagrees. In column 1, lines 37-45, Goodrum et al. disclose that the fault isolation controller is used to turn devices off by powering them off. The devices are coupled to a bus, and the faulty condition includes a bus hang condition. The watcher includes a bus timer to monitor the bus to detect the bus hang condition. The bus hang condition is present if the bus timer expires. The fault isolation controller is used to turn off the devices when the bus hang condition is detected and to turn the devices back on to test the device (wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus status signal). Further, in column 2, lines 33-37, Goodrum et al. disclose that the illegal condition occurs when a PCI signal TRDY_, STOP_, or DEVSEL_ is asserted during a bus idle condition (a received device isolation signal).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

SCOTT BADERMAN
PRIMARY EXAMINER